		STUDY MODULE D	ESCRIPTION FORM			
	f the module/subject gn of systems w	ith FPGA	Code 1010842131010842439			
Field of study Electronics and Telecommunications Elective path/specialty			Profile of study (general academic, practical general academic Subject offered in:			
Multimedia and Consumer Electronics			Polish	elective		
Cycle of	f study:		Form of study (full-time,part-time)			
Second-cycle studies			full-time			
No. of h	ours			No. of credits		
Lectur	re: 1 Classes	s: - Laboratory: 2	Project/seminars:	- 2		
Status c	-	program (Basic, major, other)	(university-wide, from another	,		
		other	fr	om field		
Educatio	on areas and fields of scient	ence and art		ECTS distribution (number and %)		
techr	nical sciences			2 100%		
Resp	onsible for subje	ect / lecturer:				
dr inż. Adam Łuczak email: aluczak@multimedia.edu.pl tel. +48 6653840 Faculty of Electronics and Telecommunications ul. Piotrowo 3A 60-965 Poznań						
		s of knowledge, skills an	d social competencies	:		
	Has a basic knowledge about a trends in the development of FPGA devices.					
1	Knowledge	Has sufficient knowledge to design specialized digital circuits for FPGA devices.				
		Has basic knowledge about communication interfaces.				
		Has knowledge about the basic streams).		of digital circuits (automatic,		
		Has a general knowledge in area	,			
2	Skills	Is able find a required information in the literature and other sources, can integrate the information, can interpret them. Can describe the elements of a digital system using the Verilog language.				
		Can test and verify of a digital ci	• • • •	g language.		
		Can test and verify a digital mod				
		Can exploit the known design te		cuit.		
		Has the ability to exploit modern platform.	tools of the design and synthe	esis of digital circuits for FPGA		
3	Social competencies	Demonstrate responsibility for de	esigned electronic and telecom	nmunication systems		
Assu	mptions and obj	ectives of the course:				
Architecture of programmable FPGA programmable hybrid systems (CPU ARM + FPGA matrix). Construction and how to design systems SoC (System-on-Chip). Advanced language features Verilog and SystemVerilog language introduction: advanced simulation methods, compilation and synthesis systems, sample projects selected algorithms.						
		mes and reference to the				
Know	vledge:					
1. Student has a basic knowledge about hybrid FPGA devices - [K_W_01]						
2. Student has a basic knowledge about design SoC systems - [K_W_01]						
3. Student has a basic knowledge about fast communication interfaces (HD-SDI, SATA, PCI-E) - [K_W_01]						
Skills:						
1. Can describe complex digital system as a hierarchy of modules using Verilog language [K_U16]						
 Can correctly determine the parameters of the interface between the two frequency domains [K_U16] Can acquire data from the literature and other sources, can integrate the information, make their interpretation, as well as 						
	3. Can acquire data from the literature and other sources, can integrate the information, make their interpretation, as well as formulate and to justify opinions [K_U01 K_U02 K_u08]					

Social competencies:

- 1. Can see and analyze development of design techniques [K_K01]
- 2. Ability of self-learning (textbooks, computer programs) [K_K02]
- 3. Knowing the responsibility for the electronic and telecommunication systems being designed [K_K03]

Assessment methods of study outcomes

Individual projects, written or oral exam.

Course description

Development and trends in FPGA for example, the latest of programmable FPGA from Xilinx - integrated Artix-7, Kintex-7, Virtex-7, new technologies, "Stacked Silicon Interconnect Technology", "Multi-Gigabit Serial I / O".

Hybrid integrated programmable FPGA - (+ ARM processor programmable matrix).

Frequency domain - the problem of the transmission of data between domains, industrial recommendations, synchronization systems, source synchronous interface.

High Speed ??Interfaces I / O modules with use of gigabit-GTP, GTX, GTH standard HD-SDI, SATA, PCI-E. SerDes circuits in standard HDMI FlatLink.

Systems on a Chip (SoC).

Programming Languages ??- Verilog, VHDL, Systec, SystemVerilog. Principles of good programming, listing just described. Methods and tools for simulation and synthesis for FPGA designs - generate EDIF files, partition design, TCL scripting language.

Examples of effective implementation of certain algorithms (DCT conversion, color space conversion RGB> YUV, square root, multiplication, complex, floating point operations) for FPGA.

Basic bibliography:

1. Węgrzyn M., Barkalov A.,?Design of Control Units with Programmable Logic?. Zielona Góra 2006.

2. Skahill K., ?Język VHDL?, WNT, Warszawa 2001

Additional bibliography:

1. Woods R. McAllister J., Yi Y. Lightbody G. ?FPGA-based Implementation of Signal Processing Systems?, Wiley, 2008.

- 2. Palnitkar S., ?Verilog HDL (2nd Edition)?, Prentice Hall Professional, 3 mar 2003,
- 3. Kilts S., ?Advanced FPGA DESIGN?, Wiley 2007.

Result of average student's workload

Activity	Time (working hours)	
1. Activities that require personal contact with an academic teacher	90	
2. Reading literature (manuals, directories)	15	
3. Preparation for the lab	10	
4. Preparation for the exam	10	
Student's wo	rkload	
Source of workload	hours	ECTS
Total workload	60	2
Contact hours	45	1
Practical activities	15	1